



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/164,898	10/01/1998	JAMES AKIYAMA	42390.P3373	7208

7590 06/14/2002

JAMES H SALTER
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
7TH FLOOR
LOS ANGELES, CA 90025

EXAMINER

VITAL, PIERRE M

ART UNIT	PAPER NUMBER
----------	--------------

2186

DATE MAILED: 06/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.
09/164,898

Applicant(s)
Aklyama, James

Examiner
Pierre Vital

Art Unit
2186

— The MAILING DATE of this communication appears on the cover sheet with the correspondence address —

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on May 22, 2002

2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 19-37 is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 19-37 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

4) ☐ Interview Summary (PTO-413) Paper No(s). _____

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

5) ☐ Notice of Informal Patent Application (PTO-152)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

6) ☐ Other:

Art Unit: 2186

DETAILED ACTION

Continued Examination Under 37 C.F.R. 1.114

1. A request for continued examination under 37 C.F.R. 1.114, including the fee set forth in 37 C.F.R. 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 C.F.R. 1.114, and the fee set forth in 37 C.F.R. 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 C.F.R. 1.114. Applicant's submission filed on May 22, 2002 has been entered.

Response to Amendment

2. This Office Action is in response to applicant's communication filed May 22, 2002 in response to PTO Office Action mailed April 25, 2002. The applicant's remarks and amendment to the specification and/or the claims were considered with the results that follow.

3. Claims 19-37 have been presented for examination in this application. In response to the last Office Action, claims 19, 28 and 35 have been amended. No claims have been canceled or added. As a result, claims 19-37 are now pending in this application.

4. The rejection of claims 19-22, 24-31 and 33-36 under 35 U.S.C. § 103 (a) based on the Labatte (5,913,057) reference has been withdrawn due to the amendment filed May 22, 2002, as being owned by the same assignee of the present invention.

Art Unit: 2186

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 19-22, 24-31 and 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US5,905,910) and Jones et al. (US5,619,723).

As per claims 19, 25, 28 and 35, Anderson teaches a system for multi-threaded disk drive interrupt processing wherein the first and second disk drives 110 and 112 may be integrated device electronics (IDE) disk drives wherein the disk drive itself contains many of the required interface components; with IDE disk drives, a single interface coupled to the bus system 108 is capable of operating multiple IDE disk drives [Col.5, lines 28-33]; it is the instructions in the BIOS 106 itself that controls the positioning of the read/write head in the first disk drive 110 and the second disk drive 112 [Col.8, lines 12-15]; in the disk striping embodiment of the system 100, a data file is apportioned into blocks that are alternately stored (interleaved) on the first drive 110 and the second drive 112; the system 100 advantageously allows the BIOS 106 to issue commands to both the first disk drive 110 and the second disk drive 112 to allow each of the first and second disk drives to simultaneously (parallel) perform the consuming task of positioning the read/write head at the proper location on the disk drive [Col.8, lines 62-67; Col.9, lines 1-3]; with respect to the disk striping aspect of the system 100, the operating system behaves if there is a

Art Unit: 2186

single disk drive (single physical drive) rather than the first disk drive 110 and the second disk drive 112 [Col.7, lines 60-63].

However, Anderson fails to specifically teach an interface connected to the system bus and receiving requests from the BIOS; and a striping controller connected between said first and second disk drives and said interface, said striping controller causing data being communicated between said system bus and said first and second drives to be substantially read or written in parallel.

Jones discloses an interface connected to a system bus and communicating with the BIOS [Fig.1; Col.14, Lines 24-31; col.23, lines 15-25]; a striping controller connected between said first and second disk drives and said interface [Col.14, Lines 28-33], said striping controller causing data being communicated between said system bus and said first and second drives to be substantially read or written in parallel [Col.16, Lines 32-35].

It would have been obvious to one of ordinary skill in the art, having the teachings of Anderson and Jones before him at the time the invention was made, to modify the system taught by Anderson to include a controller for controlling striping of the disks, the controller causing data being communicated between said system bus and said first and second drives to be substantially read or written in parallel and an interface receiving requests from a BIOS via a system bus because it would have improved system performance by allowing reconstruction of data without any down time.

Art Unit: 2186

As per claims 20, 29 and 36, Anderson teaches interleaving data so that even sectors are accessed on the first disk drive and odd sectors are accessed on the second disk drive [col.4, lines 16-30].

As per claims 21 and 30, Anderson discloses data being transmitted between the system bus and the first and second disk drives is subdivided into a plurality of sequential blocks [col.8, lines 62-65].

As per claims 22 and 31, Anderson teaches the first disk drive is accessed for every other block of data and the second disk drive is accessed for the remaining blocks [col.11, lines 35-50; col.12, lines 3-23].

As per claim 34, Anderson discloses a control logic receives a system request intended for a single physical drive from the system bus [Col.7, lines 60-63].

As per claims 24 and 33, Anderson discloses mapping bits of the system request to a first system request data structure to be supplied to the first disk drive and a second system request data structure to be supplied to the second disk drive [Col.8, lines 54-61].

As per claim 26, Anderson discloses receiving an IDE request at a striping controller [col.8, lines 65-67].

Art Unit: 2186

7. Claims 23 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US5,905,910) and Jones et al. (US5,619,723) and further in view of Jenkins (US4,047,157).

As per claims 23 and 32, the combination of Anderson and Jones teach the claimed invention as detailed above in the previous paragraphs. However, neither Anderson nor Jones specifically teach that the system request includes a sector bit string, a head bit string, a track bit string and a driver bit as recited in the claims.

Jenkins teaches a controller for use in a data processing system wherein in the track/sector register 146 Track Address and Sector Address bit positions identify, respectively, the track and sector on a disk to be involved in a transfer; in a fixed-head unit, the Track Address bits identify a specific head [Col.20, lines 38-42]; a Write signal, produced in response to the function bits, enables drivers 297 to load data onto the data set 101 [Col.26, lines 26-28].

It would have been obvious to one of ordinary skill in the art, having the teachings of Anderson and Jones and Jenkins before him at the time the invention was made, to modify the system taught by Anderson and Jones to include sector bit string, head bit string, track bit string and driver bit in the system request because it would have improved processing speeds and memory access times by providing the system identification information for the physical location on the drive from which the data file will be read or written as taught by Jenkins.

Art Unit: 2186

8. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US5,905,910) and Jones et al. (US5,619,723) and further in view of Mizuno et al. (US5,608,891).

As per claim 37, the combination of Anderson and Jones teach the claimed invention as detailed above in the previous paragraphs. However, neither Anderson nor Jones specifically teach a first FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a first storage device and a second FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a second storage device as recited in the claims.

Mizuno discloses a first FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a first storage device and a second FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a second storage device [col.17 , lines 8-28].

It would have been obvious to one of ordinary skill in the art, having the teachings of Anderson and Jones and Mizuno before him at the time the invention was made, to modify the system taught by Anderson and Jones to include a first FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a first storage device and a second FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a second storage device because it would have improved system performance by reducing the time required for temporarily storing write data in memory and then exclusive oring the data to find redundant data as taught by Mizuno.

Art Unit: 2186

Response to Arguments

9. Applicant's arguments filed October 9, 2001 have been fully considered but they are not persuasive. As to the remarks, Applicant asserted that:

The prior art of record does not teach or suggest an interface coupled to a system bus that receives drive requests from a BIOS via a system bus.

Examiner respectfully traverses Applicant's arguments. Examiner would like to emphasize as in the Office Action mailed March 27, 2002 (Paper No. 17) that the system of Jones discloses an interface coupled to a system bus that receives drive requests from a BIOS as claimed by Applicant. In fact, Jones teaches a system that comprises a bus interface 108 coupled to a system bus 109 and to a microcontroller CPU 102 with embedded ROM 104 (where the BIOS is stored) and RAM 106 as detailed in column 23, lines 15-18.

It is well known in the art that the BIOS is stored in nonvolatile memory such as read only memory (ROM). It is also well known that the BIOS memory (i.e., ROM) stores a sequence of instructions (sometimes referred as the BIOS) which allows the processor to input data from and output data to (i.e., processing requests) to input/output devices (i.e., disks).

Access to the disk drives is via IDE commands sent to the disk controller by the IDE driver within the BIOS. The most popular interface system to a hard disk drive for a personal computer is commonly known as an intelligent disk electronics, i.e., IDE interface. One major advantage of the IDE disk drive is that the drive is compatible with the basic input/output system

Art Unit: 2186

(BIOS) included in most commonly used operation system for the personal computers. Therefore no additional driver is required when the IDE disk drive is added on to a personal computer whether the operation system is a disk operation system (DOS) or a Window 3.X.

As seen in Fig. 1, the ROM where the BIOS is stored is connected to the bus interface 108 through the system bus 109. It is not clear, based on Applicant's arguments, what other possible way than the system bus that the interface can communicate (i.e., receive drive requests) with the BIOS. Instructions or requests are issued from the BIOS to the processor 102 which communicates to the bus interface 108 via the system bus 109 as claimed by Applicant. Therefore, an interface coupled to a system bus that receives drive requests from a BIOS via a system bus is well known in the art and does not constitute the novelty of Applicant's invention.

Conclusion

10. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach an interface coupled to a system bus that receives requests from a BIOS.

Art Unit: 2186

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Monday to Friday 8:30 A.M. to 6:00 P.M., alternate Fridays off.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are:

After Final (703)746-7238, Non-Official (703)746-7240 and Official (703)746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Pud
Pierre M. Vital

June 11, 2002


MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100